AME Design Rules for DragonFly® IV

The design rules are not technical limitations of the system, but process parameters to ensure a high yield

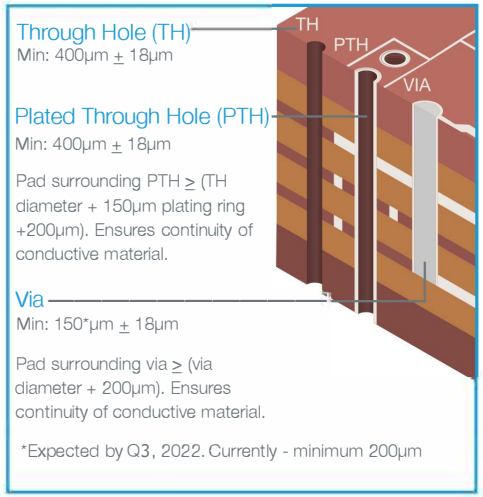
NANODIMENSION
Electrifying Additive Manufacturing®

Min Trace Width 75µm ± 9µm

Min Electrical Clearance / Space

Clearance/Space	Trace Thickness
100µm ± 9µm	17µm - 50µm
150µm ± 9µm	50µm - 100µm

Minimum PTH/Via release/clearance: 250µm



Through Hole (TH)
Min: 400µm ± 18µm

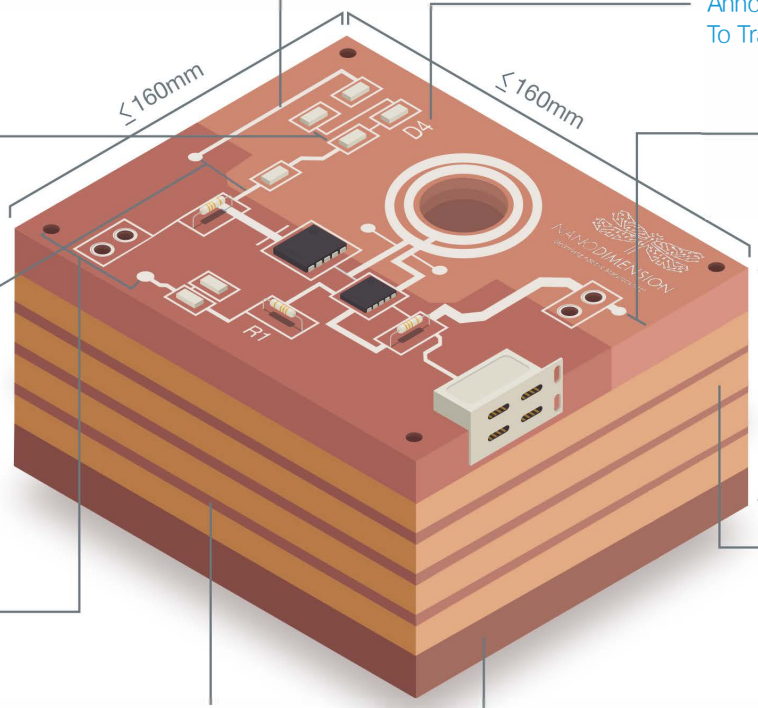
Plated Through Hole (PTH)
Min: 400µm ± 18µm

Pad surrounding PTH ≥ (TH diameter + 150µm plating ring +200µm). Ensures continuity of conductive material.

Via
Min: 150*µm ± 18µm

Pad surrounding via ≥ (via diameter + 200µm). Ensures continuity of conductive material.

*Expected by Q3, 2022. Currently - minimum 200µm



Annotation Clearance
To Trace > 180µm

Edge Spacing
0.5mm (When no edge plating)

0.7mm ≤ Thickness ≤ 3mm ±5%

Minimum Prepreg Above Layer

Signal/plane thickness ± 5%	Min Prepreg above layer
17 - 34µm	50µm
35 - 69µm	75µm
70 - 99µm	125µm
100µm	150µm

Signal / Plane Layer Thickness
Min: 17µm, 6µm steps
up to 100µm

Top / Bottom Solder Mask Thickness
50µm